1 Overview of FC Oncore B Instant GPS Module

1.1 Description

FC Oncore Version B is an extremely small high performance GPS receiver, capable of weak signal operation. Based around the Sirf GSCi-5000 Single Chip GPS Navigation Engine and SiRF provided firmware. It contains all the functional blocks to perform autonomous, MS-Based or MS-Assisted GPS operations. This comprehensive, self-contained GPS receiver is designed to allow fast, cost effective and easy integration of GPS functionality into new and existing platforms. FC Oncore supports either a passive or an active antenna input and either UART or SPI serial communications.

Element	Feature	Benefit
Tiny size	12.0x 16.6x 2.5 mm	Low impact on host product size
Autonomous capable	Simple serial host Interface	No real time demands on your host application
Correlators	8192	Good initial acquisition and low power consumption
Fast Time Resolution	Resolve time from GPS Signal	Eliminates need for highly accurate time transfer from host application
Power Manager	Software controlled	Optimize power consumption for your application
Clock Manager	Onboard TCXO only active while position measurement active	Minimizes power 256K
20KB SRAM	Keep alive patch RAM	Load patches or code
LGA Packaging	Connector elimination	Low-cost production
Low IF Front End	Low RF Component count	Good jamming immunity
On-Chip LNA	Support Active or Passive Antenna	Design for cost flexibility
Assisted protocols	Support of Industry standard A-GPS Protocol	Simple host software integration
RoHS Compliance	Free from hazardous substances	Environmental friendly

Table 1

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1.2 Functional Diagram

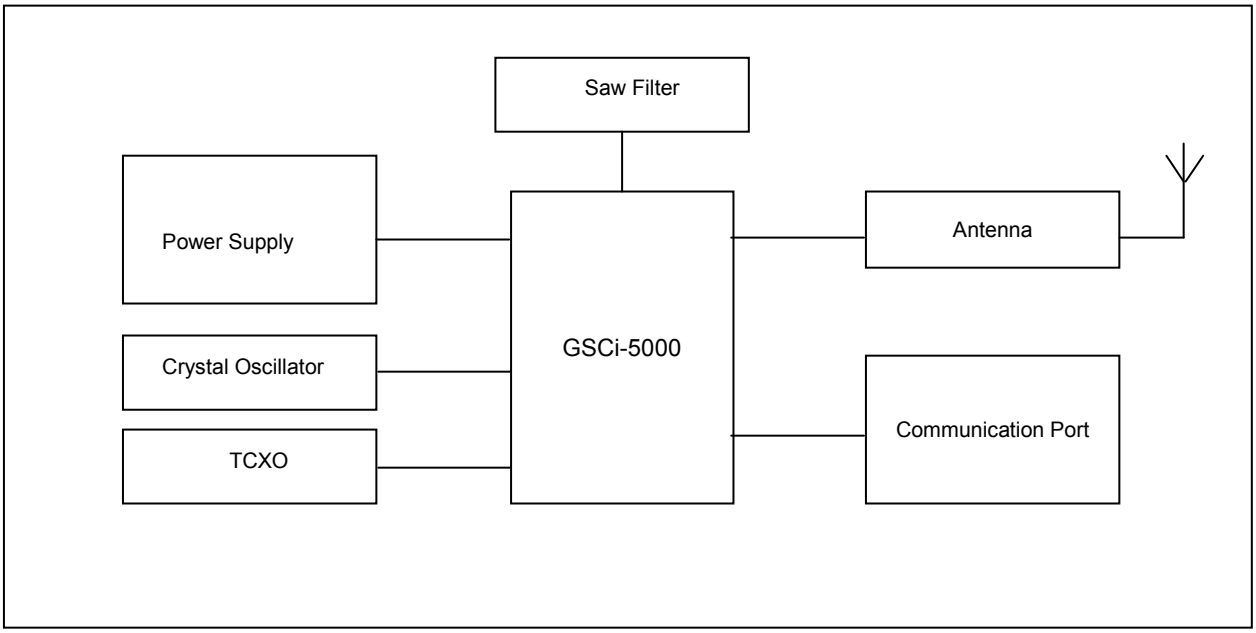


Figure 1 Functional Block Diagram

FC Oncore version B is a compact reflow-able Land Grid Array (LGA) module, built with high temperature solder. Ideal for high volume production, modules are supplied in tape and reel format ready for placement. Communication is via a SPI or UART port and minimal host interaction is required to operate autonomously. To optimize power usage device can be set to low power states SLEEP or DEEP SLEEP.

SLEEP: Typical consumption of ~ 45µA, Device can be awoken via the internal RTC timers, or by SPI or UART port activity.

DEEP SLEEP: lowest power state achieved by holding nRESET pin low, hence drawing ~5 µA of total current.

In autonomous mode, FC Oncore Version B functions as a standard GPS receiver, outputting position, velocity and time at a maximum 1 Hz update rate.
In assisted mode, a cellular network can provide A-GPS information allowing fast acquisition at low signal levels.

MS-Assisted, MS-Based and multimode operation is supported with messages based around the 3GPP RRLP/RRC specification, simplifying host driver software tasks.

1.3 Ordering Information

Device	Marking	Package	Reel Size
FC Oncore	FC Oncore X	24 Pin LGA with centre Ground pad	1000

1.4 Applicable Documents

- Data sheet GSCi-5000, ROM Release 1.2
- 103-GPS-050 Revision A, Product Requirement Specifications – FC Oncore Ver. B SPI dated March 08, 2007
- 103-GPS-051 Revision A, Product Requirement Specifications – FC Oncore Ver.B UART dated March 08, 2007
- 92-G10564A Revision AB, SiRF Instant GPS IC Interface Control Drawing dated June 16, 2006

2 System Overview

2.1 Functional Overview

The FC Oncore B solution enables easy integration of GPS location sensing into virtually any application enable location-based services, and provide Assisted-GPS (A-GPS) and autonomous GPS tracking technology.

This section outlines the host interaction with the FC Oncore software and hardware. By keeping the interface between the FC Oncore and the host processor simple, integration into any application is easily achieved.

2.2 System Block Diagram

A typical FC Oncore system may be broken down into the following hardware/software partitions.

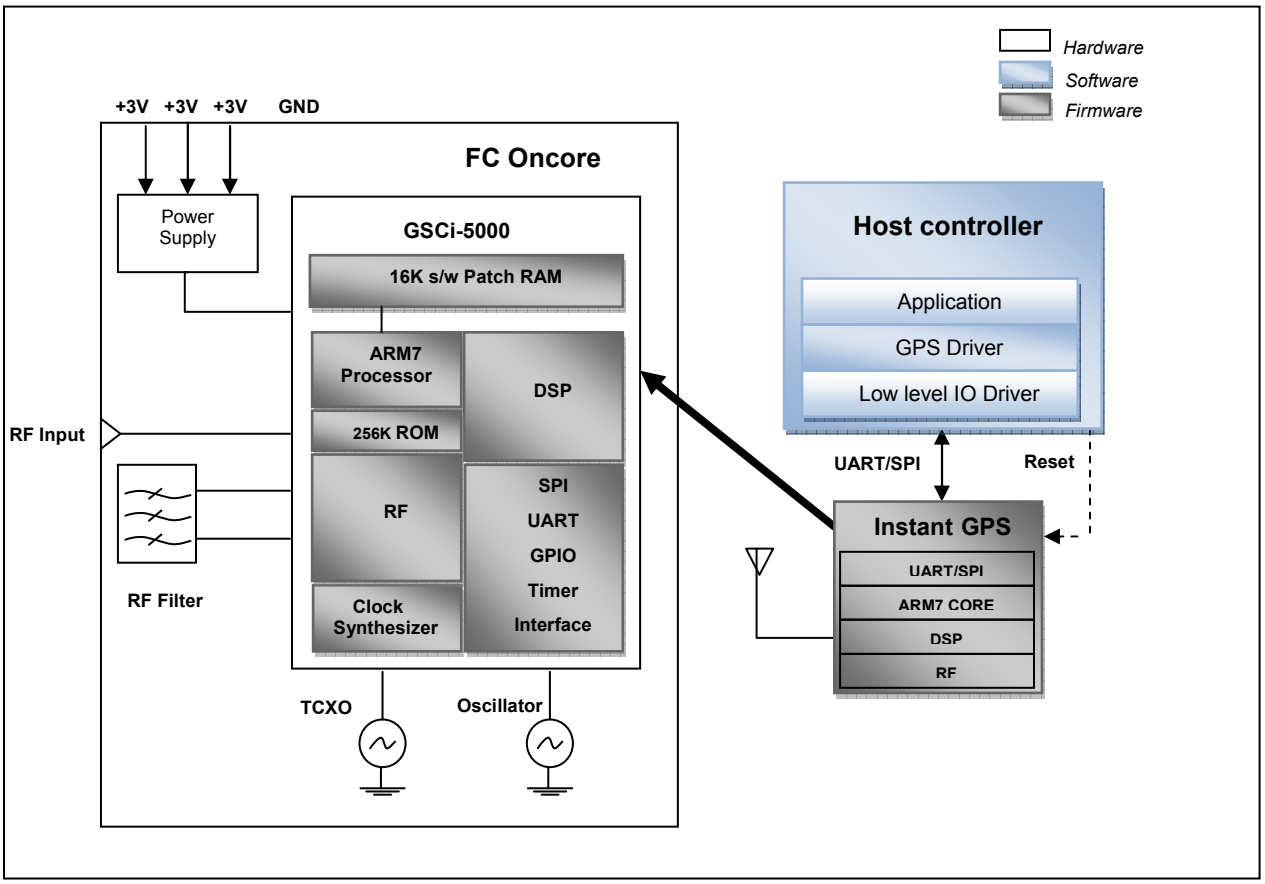


Figure 2 System Block Diagram

2.3 Host Software

Upon power up, firmware for the FC Oncore must be downloaded from the host application or host controller initialize the FC Oncore. After initialization GPS data can be provided over the serial connection in either the SiRF Instant binary protocol or the standard NMEA format

2.4 Firmware

The GSCi-5000 ROM version is a stand-alone receiver. The firmware provided will enable users to perform both Autonomous, and Assisted GPS (A-GPS). The interface is capable of either NMEA and/or SiRF instant binary output over the serial communication port.
The GSCi-5000 receives and decodes GPS signals at 1575.42 MHz It is a self-contained GPS receiver capable of producing a final position solution including full tracking and data decode capability. A patch RAM memory is available and used for software updates to the ROM version.

2.5 FC-Oncore Module

2.5.1 GSCi-5000 IC

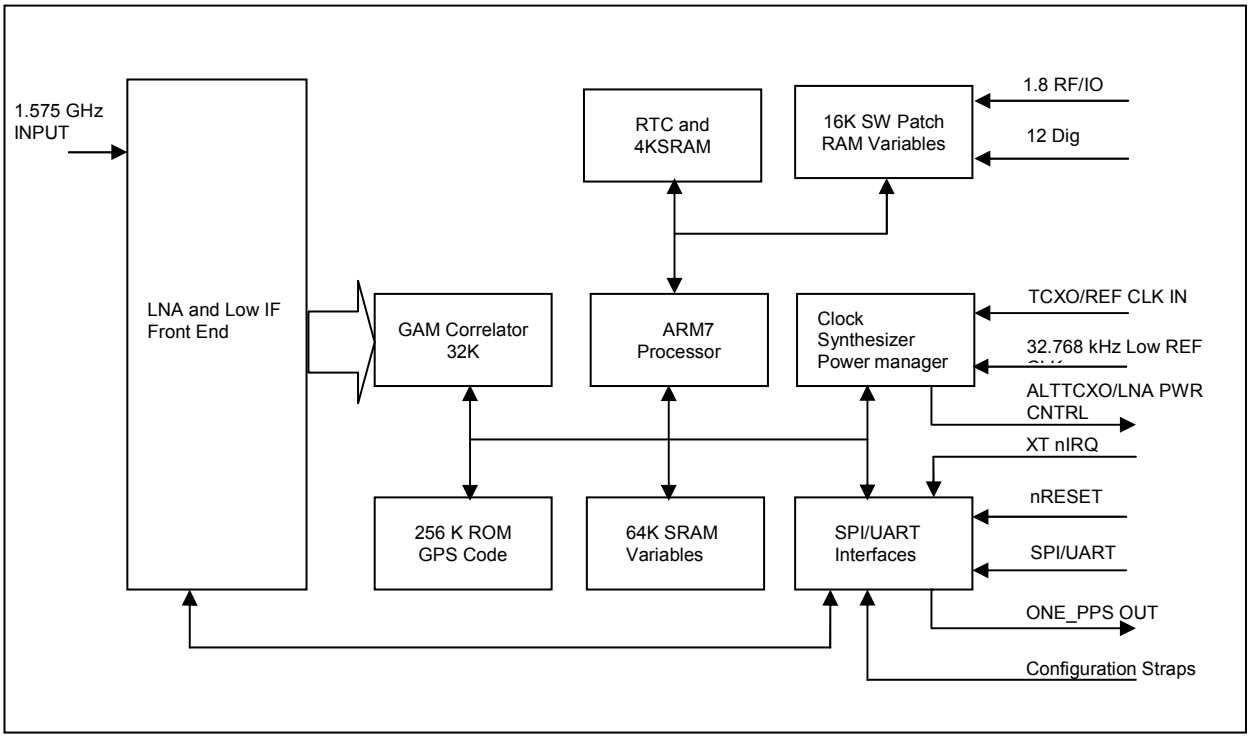


Figure 3 GSCi-5000 Functional Block Diagram

2.5.2 Integrated LNA, TCXO, 32 KHz clock and SAW filter

With an integrated LNA the FC Oncore greatly simplifies the integration of a GPS receiver into existing systems. The on-chip LNA eliminates the need for expensive active antenna circuits, increases sensitivity, and reduces the overall power consumption of the GPS receiver.

2.5.3 Serial Communications

Communication between the FC Oncore B receiver and the host processor can be accomplished through either a UART or SPI interface
The UART and Host SPI interfaces share the same connection pins of the GSCi-5000. Selection of SPI or UART mode is made using the TDI, TMS, and FDIN signals.
This receiver is configured to always be in a default slave mode.

The primary features of the UART are:
• Default baud rate 19200
• User selectable baud rates from 4800 to 57600 during normal operation. Higher speeds (~ 1 M baud) are possible during patch download.
•Two or four wire operation.

2.5.4 1PPS

Precise time keeping can be provided by the FC Oncore receiver by using the one pulse per second (1PPS) output. By using the precise time properties of the GPS system a precision timing pulse can be provided to external circuitry such as telematics devices

2.6 External System Components

- The FC Oncore reference design will require the following additional system components:

LNA in addition to the internal LNA can be used in tandem, as long as the total RF gain input into the RFA SAW filter is less than 30 dB. If the receiver is intended to be used in a RF hostile environment, or in a platform with multiple radios, then use of a low loss pre-filter and high skirt rejection post LNA SAW filter is highly suggested. This will help to minimize the risks of in-band system jamming effects.

- Low Reference Clock:

The receiver has an internal RTC oscillator circuit available to use for low power RTC timekeeping. If desired, the RTC input buffer could also be driven by an external RTC reference clock with required signal characteristics. This reference must be always be present and stable, since it is mandatory for system boot up. Therefore, proper consideration for typical RTC startup times must be addressed for the initial power up sequence. Refer to Figure 5. for more specific timing details.

- Antenna:

Performance characteristics are highly dependent on proper antenna design, placement and development. Lack of successful antenna design and integration will degrade the system performance capabilities.

2.7 Power Management

The advanced power control circuitry in the FS Oncore allows significant power savings by using frequency scaling and power domain control. This allows the FS Oncore to achieve standby currents less than 20 uA and very low power consumption during acquisition and tracking modes. General purpose outputs are provided which can additionally be used to activate external circuits.

3 Product Specifications

3.1 Receiver Specifications

Type	Single chip GPS receiver
Channels	12 channels
Correlators	8192
Frequency	1575.42 MHz
Code	C/A

3.1.1 Sensitivity (using passive antenna*)

Acquisition (assisted)	-150 dBm
Acquisition (autonomous)	-142 dBm
Tracking (autonomous)	-151dBm

*Sensitivity is the measure of the strength of the signal at which the device can receive the signal from the GPS satellites, process, and decode the signal to provide position information. Assisted mode uses information from a network which contains relevant GPS information. Autonomous mode uses only information provided from the satellites.

3.1.2 Time-to-First-Fix (TTFF)

There are three generally accepted categories for defining acquisition time, or Time To First Fix (TTFF). There are also other categories for TTFF which are defined by the manufacturer based on innovative operating modes or time keeping. The three generally accepted categories are Hot Start, Warm Start and Cold Start. Because in GPS we are trying to measure a signal with accuracy, the precision of the TXCO is important.

3.1.2.1 Hot Start

During hot start, the receiver has valid almanac, ephemeris, time and previous position data and only needs a valid time sub-frame to generate a correct position. A typical example of a hot start would be turning the receiver off for a few minutes

3.1.2.2 Warm Start

During warm start, the receiver has valid almanac and some ephemeris data, time data to within 5 minutes of universal time (UTC) and position to within 1km. The receiver needs to collect better clock and ephemeris data, but knows where to find and quickly collect one frame of the navigation message, which is 30 s long. A typical example of a warm start would be turning the receiver off for two to eight hours.

3.1.2.3 Cold Start

During cold start, the receiver has no ephemeris or almanac data and may have no time data to within 5 minutes of universal time (UTC). Coarse time data can be provided through the application if available. In this situation, the receiver must search the sky, find the satellites and decode the messages. The time to locate the satellites is strongly dependent on Correlators design and number of correlators. A typical example of a cold start would be the receiver being in a box for many days, or fresh out of the box.

3.1.2.4 TTFF, Sensitivity, Accuracy and Power Consumption

(1) Autonomous Mode		Specification	Condition
	(i) TTFF (Acquisition)		
	cold start	< 45sec 50% @ -137 dBm	0.5ppm reference oscillator uncertainty
	warm start	< 38sec 50% @ -137 dBm	
	hot start	< 5 sec 50% @ -137 dBm	
	(ii) Sensitivity	-142 dBm	Acquisition and Tracking
	(iii) Accuracy**		
	Position error at 50%	<3 m @ -137 dBm	
	Position error at 95%	<5 m @ -137dBm	
	(iv) Power Consumption	<120 mW Typ@1Hz @ -137dBm	
(2) Assisted Mode			
	(i) TTFF (Acquisition)		0.5ppm reference oscillator uncertainty
	MS Based-GSM Coarse time	< 2 sec 50% @ -139dBm*	
	MS Assisted-GSM Coarse time	< 2 sec 50% @ -139dBm*	2 sec time uncertainty, 30 km position uncertainty
	(ii) Sensitivity	-150 dBm	Acquisition
	(iii) Accuracy		
	Position error at 50%	10 m @ -139 dBm	
	Position error at 95%	25 m @ -139 dBm	
	Velocity	1m/s@-137 dBm	
	Heading	TBD	

*Assisted OT/OTOP Mode ** Static Scenario

Table 2 TTFF, Sensitivity, Accuracy and Power Consumption of FC Oncore

3.2 DC Operating Conditions

3.2.1 **Power Supply Characteristics operating Temperature**

Characteristic	Symbol	Value	Units
MAXIMUM RATING			
Analog Power Supply Voltage	VCC_RF	3.6	Volts
Digital Internal Power Supply Voltage	VDD	2.5	Volts
Digital External Power Supply Voltage	VCC_3V	3.6	Volts
OPERATIONAL LIMITS			
Analog Power Supply Voltage	VCC_RF	3 VDC±10%	Volts
Digital Internal Power Supply Voltage	VDD	2 VDC±10%	Volts
Digital External Power Supply Voltage	VCC_3V	3 VDC±10%	Volts
Operating Temperature	T_{OPR}	-30 to +75	°C
Storage Temperature	T_{STG}	-40 to +85	°C
Ambient Temperature	T_{AMB}	25 ± 5	°C
Humidity (Moisture)		85 ± 10	%RH

Table 3 Supply Characteristics

3.2.2 Digital I/O Interface

VCC_RF, VCC_3V = 3V±10%, VDD1, VDD2 = 2V±10%

Characteristic	Symbol	Parametric Over Temperature			Units
		Min	Type	Max	
Digital Interface I/Os					
Input High Voltage	V_{IH}	$0.7*V_{CC\_3V}$		$V_{CC\_3V}+0.3$	VDC
Input Low Voltage	V_{IL}	-0.3		$0.3*V_{CC\_3V}$	VDC
Input Leakage Current	I_{IL}	-1.0		1.0	uA
Output High Voltage @2ma	V_{OH}	V_{CC_3V}-0.4			VDC
Output Low Voltage @2ma	V_{OL}			0.4	VDC
Pin Capacitance			5		pF
Low Ref Clock Rise/Fall				100	nS
Low Ref Clock Hysteresis		250			mV

Table 4 Digital I/O Interface

3.3 AC Characteristics

3.3.1 Power & Reset

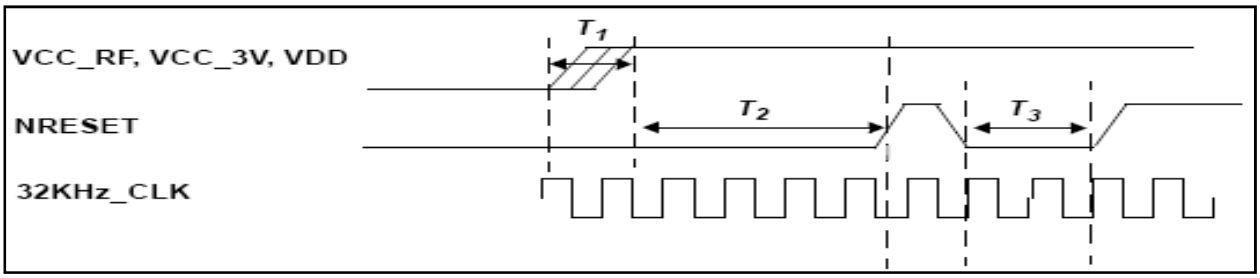


Figure 4 Reset and Power Supply Timing

Characteristic	Symbol	Parametric Over Temperature			Units
		Min	Type	Max	
Power supply rise time (All Supplies)	T1			100	ms
Power On Reset	T2	1			us
Reset Pulse Width	T3	1			us

Table 5 Reset and Power Supply Timing

3.3.2 SPI Interface

Signal	I/O	Description
MOSI_RXD0	I	Serial communication - SPI or UART. If SPI = Master-Out Slave-In. If UART = UART0 RXD.
MISO_TXD0	O	Serial communication - SPI or UART. If SPI = Master-In Slave-Out. If UART =UART0 TXD.
nPCS_RXD1	I	Serial communication - SPI or UART. If SPI, Input is Peripheral Chip Select. If UART = UART1 RXD or UART0 CTS.
SCK_TXD1	I/O	Serial communication - SPI or UART. If SPI, Input is SPI CLK input. If UART = UART1 TXD Output or, UART0 RTS output.

Table 6

SPI Clock = 312.5 kHz
Inter Byte Delay = 200 uS
Inter message Delay = 200 uS

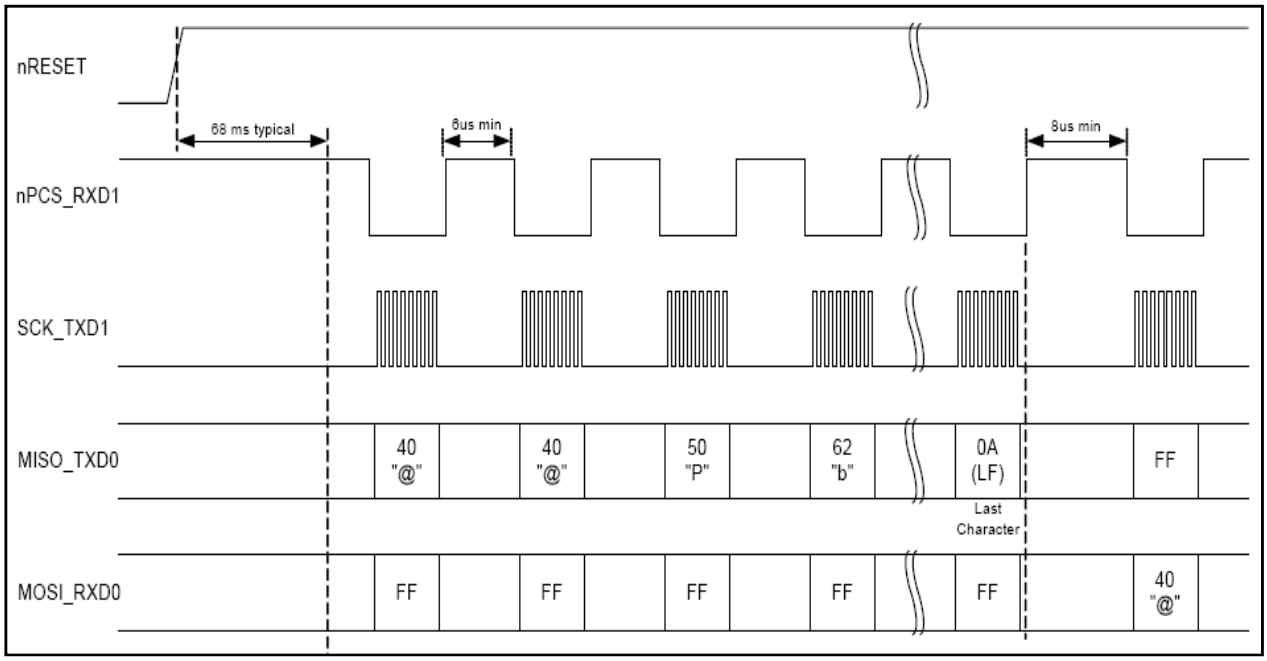


Figure 5 SPI Timing Diagram

3.3.3 UART Characteristics

Characteristic	Symbol	Min	Type	Max	Units
Baud rate		4800	19200	1,000,000(2)	baud
Word length		5	8	8	bits
Stop		1/2	-	-	bits
Parity		0	0	1(odd or even)	bits

Table 7

3.3.4 1 Pulse Per Second (onepps)

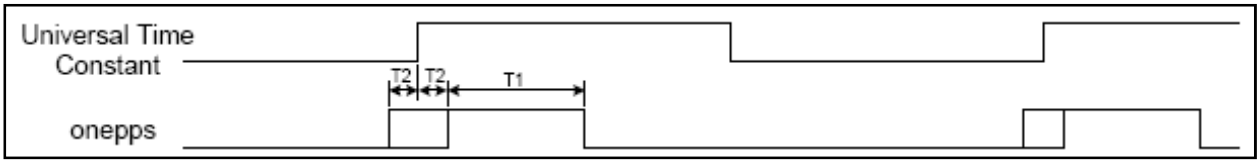


Figure 6 One PPS

Characteristic	Symbol	Parametric Over Temperature			Units
		Min	Type	Max	
Pulse Width(1)	T_1	100		300	ms
Timing Accuracy (1 sigma)	T_2		± 30		ns
Timing Accuracy (2 sigma)	T_2		± 100		ns
Timing Accuracy	T_2			1	µs

Table 8

3.4 LNA Characteristics

Characteristic	Symbol	Parametric Over Temperature			Units
		Min	Type	Max	
Input Frequency	f_{in}		1.575		GHz
Power Gain	G_P	16	18	21.5	dB
Noise figure	NF		1.3	2.5	dB
Input 1d B Compression	P_{1dB}	-24			dBm
Input Third Order Intercept(1)	IIP_3	-14			dBm
Input Return Loss(2)		6	9		dB
Output Return Loss(2)		10	18		dB

1. Based on two tones separated 1MHz centered about F_{IN}
2. Relative to 50 ohms single ended or 100 ohms differential

Table 9

3.5 Antenna Requirements

FC Oncore B IS compatible with both active and passive antenna. Passive antenna capability is enabled via the integrated LNA.

3.5.1 Active Antenna Requirements

Characteristic	Minimum Value	Typical Value	Maximum Value	Units
Antenna System Characteristic: (REFERENCE)				
Frequency	1574.40	1575.42	1576.44	MHz
Polarization	-	Right Hand Circular	-	-
Critical <!> 3 Vdc Total System Gain (Including LNA, cable loss, antenna element, and variations over temperature)	10	-	30	dBi
Filter / LNA Assembly: (Applies to all antennas regardless of cable length used.)				
Band Width ±3 dB	2	-	-	MHz
Gain Variation (at 1575.42 MHz ± 1.023 MHz)	-1.0		+1.0	dB
1 dB Compression Point (Measured at Output)	-6.0	0.0	-	dBm
Noise Figure	-	1.8	2.2	dB
Noise Figure over temperature	-	-	3.2	dB
Output VSWR	-	1.5	2.5	-
Output Return Loss	-	-	7.3	dB

Table 10

3.5.2 Passive Antenna Requirements

Characteristic	Minimum Value	Typical Value	Maximum Value	Units
Antenna Overall Characteristic:				
Frequency	1574.40	1575.42	1576.44	MHz
Polarization	-	Right Hand Circular	-	-
Gain (at Zenith)	2.0	-	-	dBi
Gain (at 0 degree elevation angle)	-3.0	-	0.0	dBi
Axial Ratio (at zenith)		3.0	6.0	dB
Output VSWR			1.5	

Table 11

3.6 Electrical Requirements for Functional Test

FACTORY	PARAMETER	TEST VOLTAGE	TOLERANCE	UNITS	NOMINAL	LOWER LIMIT	UPPER LIMIT
	Full Power Mode						
	VDD Digital Core	2.0V	± 0.2V	mA	16	10	30
	VCC_RF Analog/RF	3.0V	± 0.3V	mA	27	20	40
	VCC_3V Digital I/O	3.0V	± 0.3V	mA	1.37	0.0	3.0
	Sleep Mode						
	VDD Digital Core	2.0V	±0.2V	uA	32	10.0	60.0
	VCC_RF Analog/RF	3.0V	± 0.3V	uA	1.5	0.0	10
	VCC_3V Digital I/O	3.0V	± 0.3V	uA	40	0.0	100.0
	C/No @ - 127 dBm @25±5ºC		± 3 dB	dB	40	36	44
	Absolute Doppler			Hz		- 2350	2350

Table 12

RELIABILITY	PARAMETER	TEST VOLTAGE	TOLERANCE	UNITS	NOMINAL	LOWER LIMIT	UPPER LIMIT
	Full Power Mode						
	VDD Digital Core	2.0V	± 0.2V	mA	16	10	30
	VCC_RF Analog/RF	3.0V	± 0.3V	mA	27	20	40
	VCC_3V Digital I/O	3.0V	± 0.3V	mA	1.37	0.0	3.0
	Sleep Mode						
	VDD Digital Core	2.0V	± 0.2V	uA	32	10.0	60.0
	VCC_RF Analog/RF	3.0V	± 0.3V	uA	1.5	0.0	10
	VCC_3V Digital I/O	3.0V	± 0.3V	uA	40	0.0	100.0
	C/No @ - 127 dBm @25±5ºC		± 3 dB	dB	40	36	44
	Absolute Doppler			Hz		- 2350	2350

Table 13

4 Mechanical Requirements

4.1 Package

4.1.1 Packaging Style

24 pin LGA package with centre ground pad

4.1.2 Immersion Gold Plating

4.1.3 Termination/Component Flatness

Co planarity (from seating plane): 0.1 mm (0.004 inches) Maximum

4.1.4 Modular Component Solder

4.2 Device Pin out and Package Definitions

Pin Number	Signal	Type	Description
1	GPIO1	O	Enable/Disable TCXO
2	N/C	N/C	Future Compatibility
3	GND	I	Ground
4	GND	I	Ground
5	GND	I	Ground
6	GND	I	Ground
7	VDD	VDD	Digital Core VDD
8	VDD	VDD	Digital Core VDD
9	VCC_3V	VCC	Digital I/O VCC
10	GND	I	Ground
11	VCC_RF	VCC	Analog/RF VCC
12	GND	I	Ground
13	ANT_IN	RF I	Antenna input
14	GND	I	Ground
15	NRESET	I	Reset
16	SCK_TXD1	I/O	Serial interface bus
17	MOSI_RXD0	I/O	Serial interface bus
18	MISO_TXD0	I/O	Serial interface bus
19	NPCS_RXD1	I/O	Serial interface bus
20	1PPS	O	1pps output
21	NIRQ	I	External interrupt Input
22	32KHz CLK	O	Real Time Clock Output
23	N/C	N/C	Future Compatibility
24	N/C	N/C	Future Compatibility
25	GND	GND	Center Ground Pad

Table 14

Mechanical

Mechanical Dimension Of FC Oncore B Module

FC Oncore Ver. B, 1575.42MHz, 12x16.6x2.75mm

Following are FC Oncore B Top view, Side view and Bottom view. These views show the general dimensions of the module.

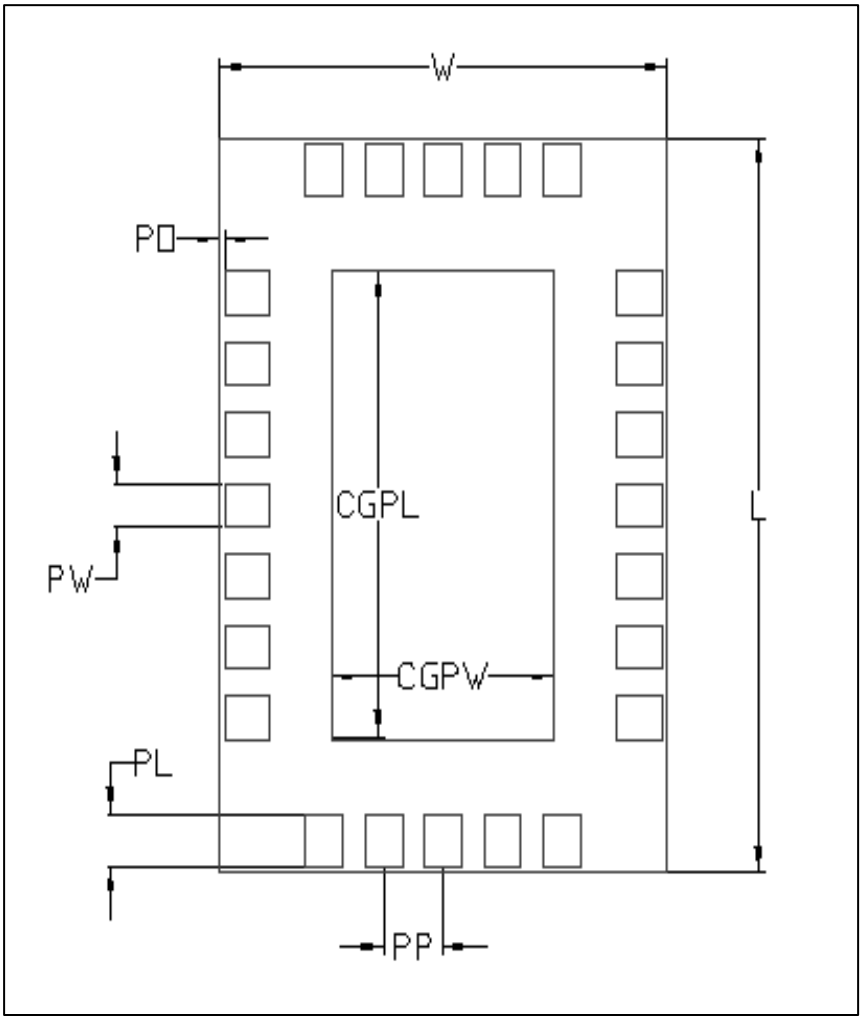


Figure 7 Top View of Bottom IO Pads

CRITICAL	DESCRIPTION	SYMBOL	UNITS	LOWER LIMIT	NOMINAL	UPPER LIMIT
[X]	Overall Body Height:	H	mm	-	2.75	2.90
[X]	Package Body Length:	L	mm	-	16.6	-
[X]	Package Body Width:	W	mm	-	12.0	-
[X]	I/O Pad Length:	PL	mm	1.1	1.2	1.3
[X]	I/O Pad Width:	PW	mm	0.9	1.0	1.1
[X]	I/O Pad Pitch:	PP	mm	1.5	1.6	1.7
[X]	I/O Pad Offset:	PO	mm	0.027	0.127	0.227
[X]	Center Gnd Pad Length:	CGPL	mm	10.5	10.6	10.7
[X]	Center Gnd Pad Width:	CGPW	mm	5.9	6.0	6.1

Table 15

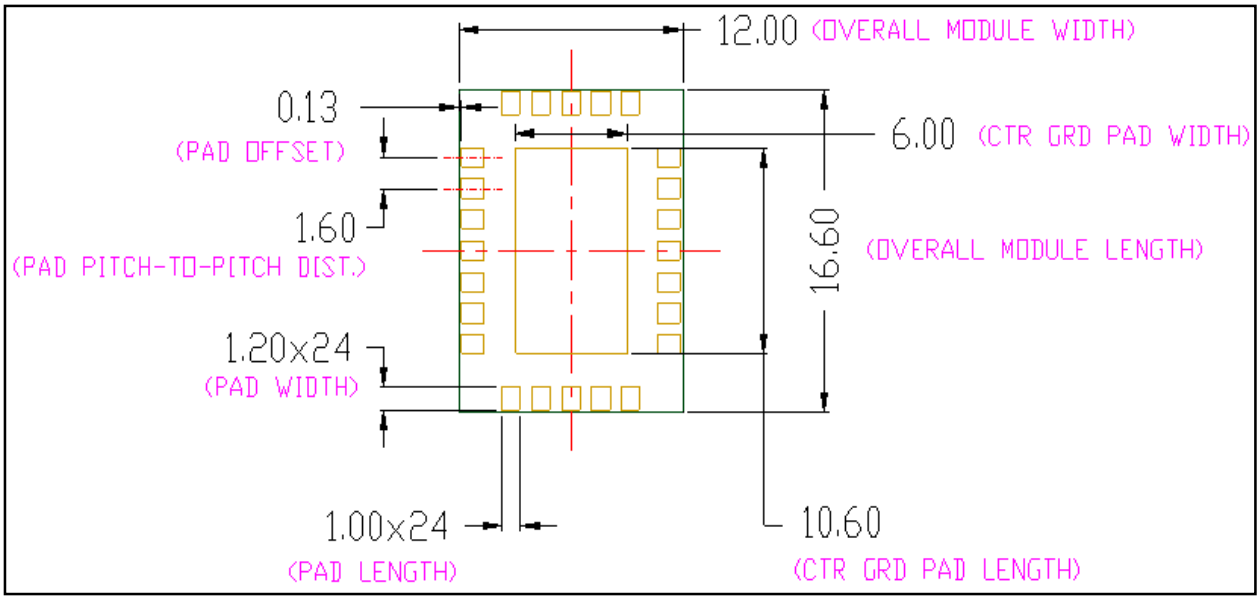


Figure 8 Bottom View

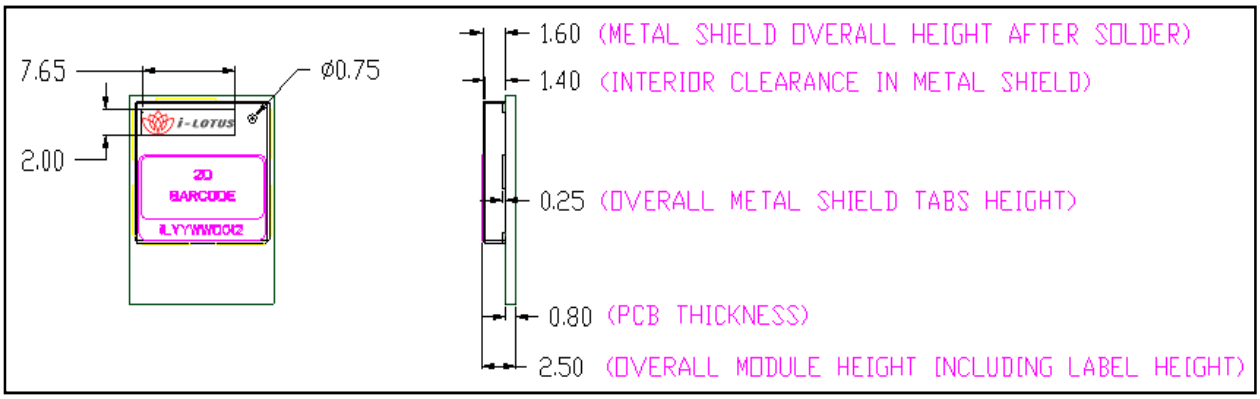
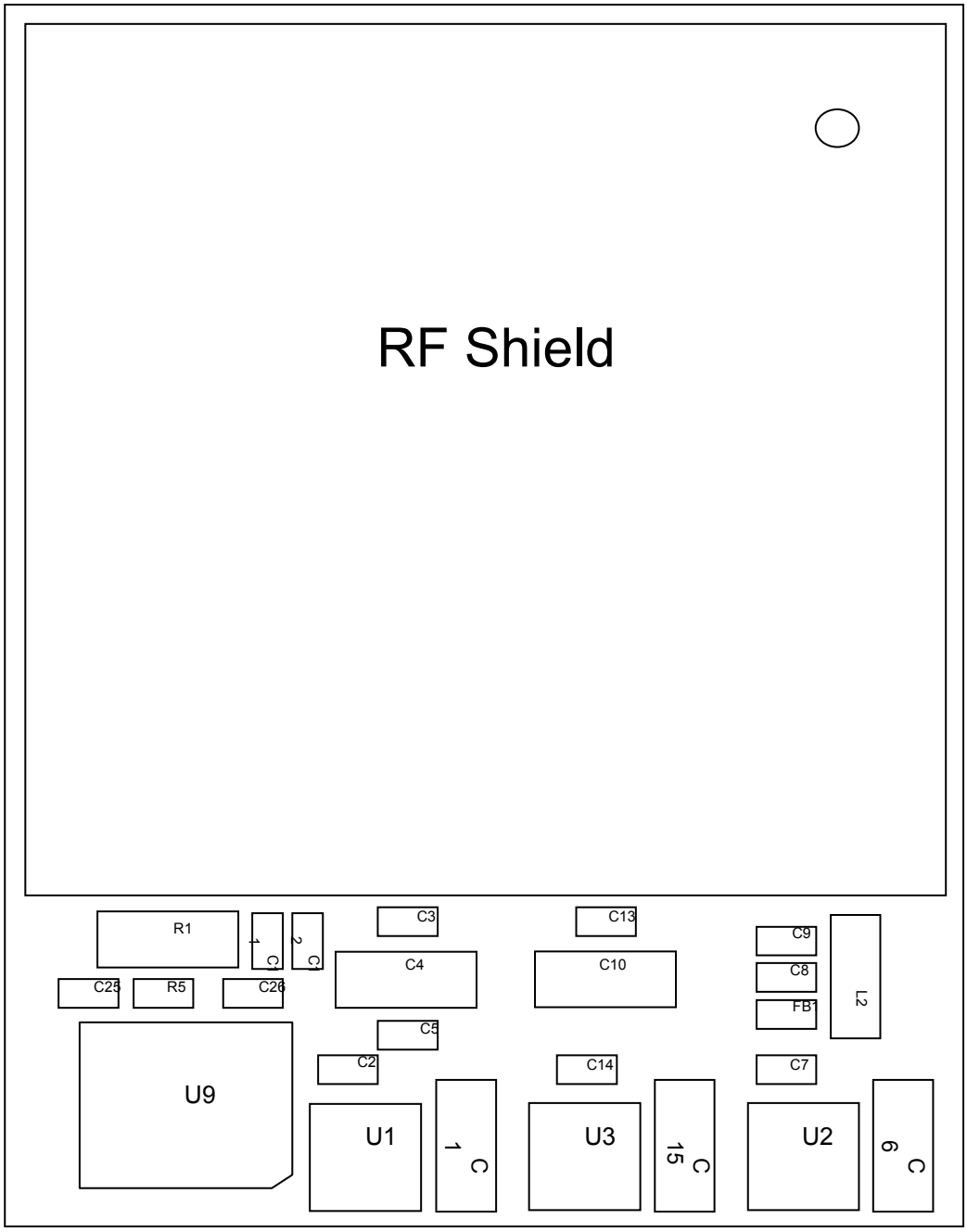


Figure 9 Top and Side View

4.3 Tape and Reel Packaging

- Tape and Reel Packaging with the following conditions:
- Tape width: 32 mm +0.3 / -0.1mm
- Tape pitch : (part to par)t: 16 mm +/- 0.1mm
- Pocket dimensions: Width = 12.5 +/-±0.1mm Length = 17 ±+/-0.1mm Depth = 3.3 +/-±0.1mm
- Component orientation: Parts shall be oriented with the pad one side closest to the tape's round sprocket holes on the tape's trailing edge.
- reel diameter: 330 mm (13 inch)

- Overall thickness: 0.30 ±0.05mm.
- Material: High Impact Polystyrene, Conductive, Black.


RF Shield
R1
C1
C3
C13
C9
C4
C10
C8
C25
R5
C26
FB1
L2
C5
C2
C14
C7
U9
U1
U3
U2
C 1
C 15
C 6

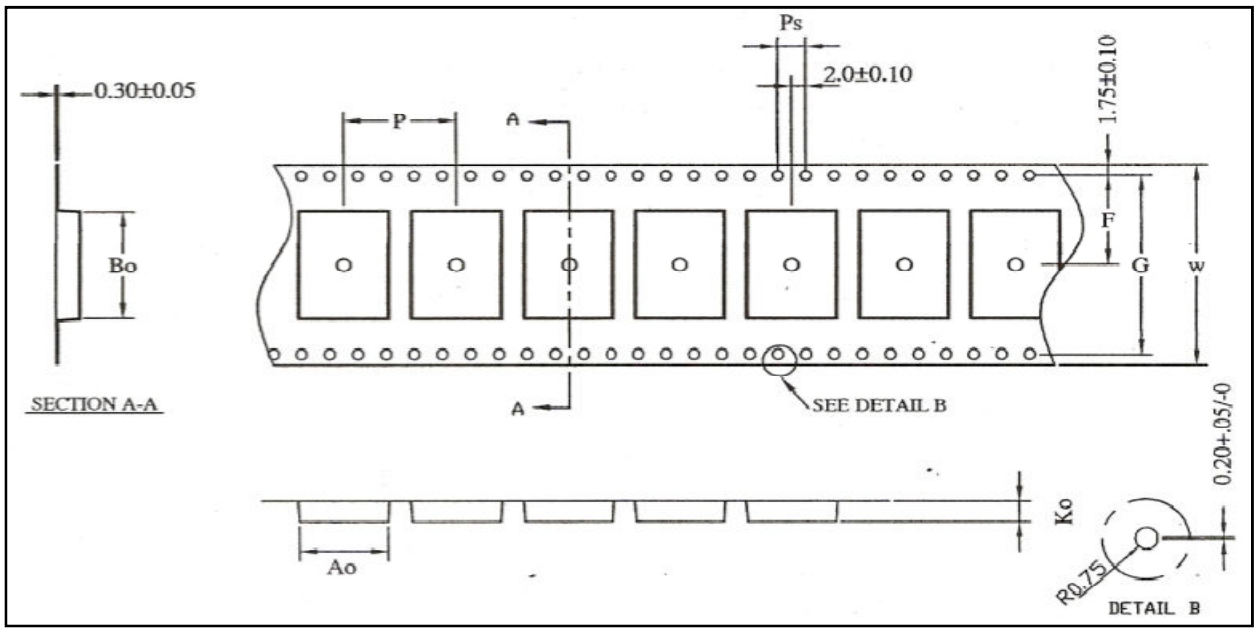


Figure 10 Tape and Reel Packaging

Dimensions	W	P	Ao	Bo	Ko	Ps	F
SPECS' Nominal	32.00	16.00	12.50	17.00	3.30	4.00	14.20
Tolerance	±0.30	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10

Table 16